Nintendo DS/DSi Enhanced/DSi Game Card Manual

Version 2.02

The content of this document is highly confidential and should be handled accordingly.

TWL-06-0019-001-B
Released: October 29, 2009

Confidential

Table of Contents

Tables

Figures

Revision History

Version	Revision Date	Description
2.02	2009/10/21	Changed logo.
2.01	2009/10/13	Added information about 4-gigabit ROM. Changed description of usage restrictions with regard to memory capacity limits. Added comment about TWL extended memory start address to section 2.1.2 Memory Map. Changed description of 1-megabit EEPROM data storage periods in section 2.2.1 Lineup. Added 16- and 64-megabit flash to the table. Deleted description of 32-megabit flash. Added description of time needed for writes and deletes on 64-megabit flash.
2.00	2008/10/07	Added information about TWL. Deleted section 2.1.2 ROM Registration Data. Now Memory Map is section 2.1.2. Deleted 2Gbit memory chip from section 2.1.2 Memory Map. Added 1Mbit to EEPROM in section 2.2.1 Lineup.
1.05	2008/02/20	Changed the description of 8-Mbit flash in section 2.2.1 Lineup.
1.04	2008/02/19	Added information about 2-Gbit ROM. Added a description about flash memory of 8 Mbit or larger to section 2.2.1 Lineup. Deleted FRAM from section 2.2.1 Lineup.
1.03	2006/12/14	Revised section 2.1.2 ROM Registration Data. Added a description of the difference in manufacturer codes. Added a specific market region for China and Korea. Changed the ROM version in figures and changed the color separation from GEN to RSF.
1.02	2006/06/19	Overall document: • Added information about 1-Gbit ROM. In section 2.1.2 ROM Registration Data: • Added items about reserved memory region: reserved region → ARM9/ARM7 module, parameter addresses • Different colors are used to indicate different methods of setting data In section 2.2.1 Lineup: • Changed the guaranteed number or writes and the time required to write for the 4-Mbit flash memory • Added 8-Mbit to flash memory
1.01	2005/10/17	In section 2.2.1 Lineup: • Changed the EEPROM data storage period from 40 years to 10 years. • Deleted mention of a scheduled release of 512-Kbit EEPROM in the second half of 2005. It is available now. • Added 4-megabit flash memory. • Deleted mention of a scheduled release of FRAM in the second half of 2005. It is available now (consultation required regarding delivery time). • Changed the number of guaranteed rewrites.
1.00	2005/07/01	Initial version.

1 Introduction

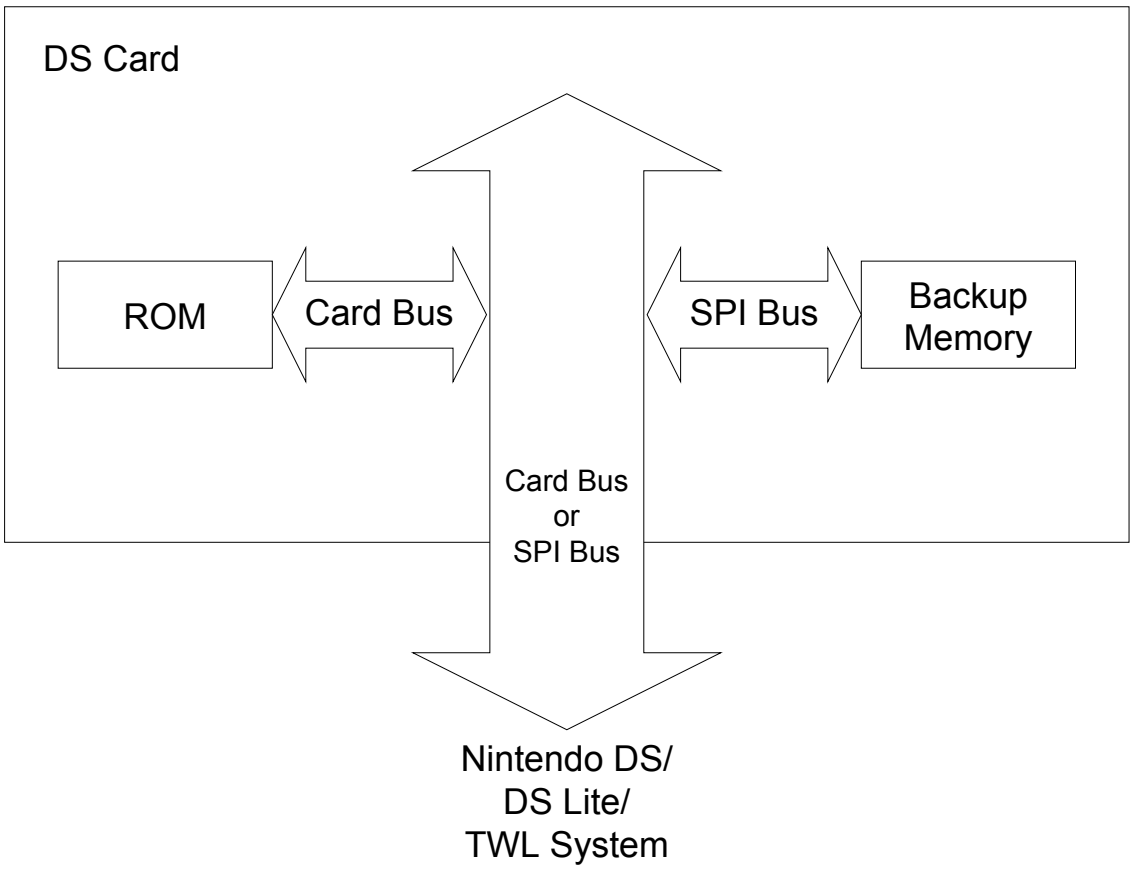
This manual describes the following Game Cards.

- Nintendo DS Game Card ("DS Card")
- Nintendo DSi Enhanced Game Card ("TWL-Enhanced Card")
- Nintendo DSi Game Card (TWL Card")

1.1 Block Diagram

Figure 1-1 shows the block diagram for the Game Card.

Figure 1-1 Card Block Diagram



2 Composition

The Game Card consists of the read-only memory (ROM) and the backup memory.

2.1 ROM

2.1.1 Types of ROM

There are two types of ROM: mask ROM and one-time PROM. The `makerom/makerom.TWL` settings file (ROM specification file) specifies the kind of ROM image that will be created. In addition,

- `makerom` in NITRO-SDK version 2.1 and earlier always creates mask ROM.
- Only the mask ROM can be selected for a 64-megabit capacity ROM.
- Support for the mask ROM is not planned for ROMs whose capacity is 1 gigabit or larger.
- For the TWL-Enhanced Card and TWL Card, only the one-time PROM type can be selected, regardless of capacity.

Features of the two types of ROM are shown in Table 2-1 and Table 2-2.

Table 2-1 Features of Each ROM Type (DS Card ROM)

	Mask ROM	One-Time PROM
Transfer Rate	5.99 MB/sec	1.52 MB/sec
Capacity	64 megabits 128 megabits 256 megabits 512 megabits	128 megabits 256 megabits 512 megabits 1 gigabit 2 gigabits 4 gigabits
Page Size	512 bytes	
Feature	Fast transfer rate	Short delivery times for repeat deliveries

Table 2-2 Features of Each ROM Type (TWL-Enhanced Card/TWL Card ROM)

	One-Time PROM
Transfer Rate	1.52 MB/sec
Capacity	256 megabits 512 megabits 1 gigabit 2 gigabits 4 gigabits
Page Size	512 bytes
Feature	Has region that only a TWL unit can read

Notes on transfer rate:

- These theoretical values exclude overhead.

  Although the transfer rate depends on the program, the difference between transfer times in the program will not be as large as the difference between the transfer rates shown in Table 2-1.
- If one-time PROM is specified for the RSF, the production could use the one-time PROM as well as the mask ROM. However, the transfer rate will always be that of the one-time PROM.

Capacity limits:

Table 2-3 Features of Each ROM Type (TWL-Enhanced Card/TWL Card ROM)

ROM Capacity	Compatible Cards	Use-Forbidden Region
64 megabit	DS Cards	
128 megabit	DS Cards	
256 megabit	DS Cards / TWL-Enhanced Cards / TWL-Exclusive Cards	
512 megabit	DS Cards / TWL-Enhanced Cards / TWL-Exclusive Cards	
1 gigabit	DS Cards / TWL-Enhanced Cards / TWL-Exclusive Cards	Last 20 megabits
2 gigabit	DS Cards / TWL-Enhanced Cards / TWL-Exclusive Cards	Last 40 megabits
4 gigabit	DS Cards / TWL-Enhanced Cards / TWL-Exclusive Cards	Last 83 megabits

- Be sure to fill the use-forbidden region with `0xff`. Access to this region is also prohibited.

TWL-Enhanced Cards:

- There is a region in the TWL-Enhanced Card ROM that can be read with a TWL unit but not with a DS unit. See section 2.1.2 Memory Map for details.

2.1.2 Memory Map

The memory map differs according to the Game Card type.

2.1.2.1 DS Card

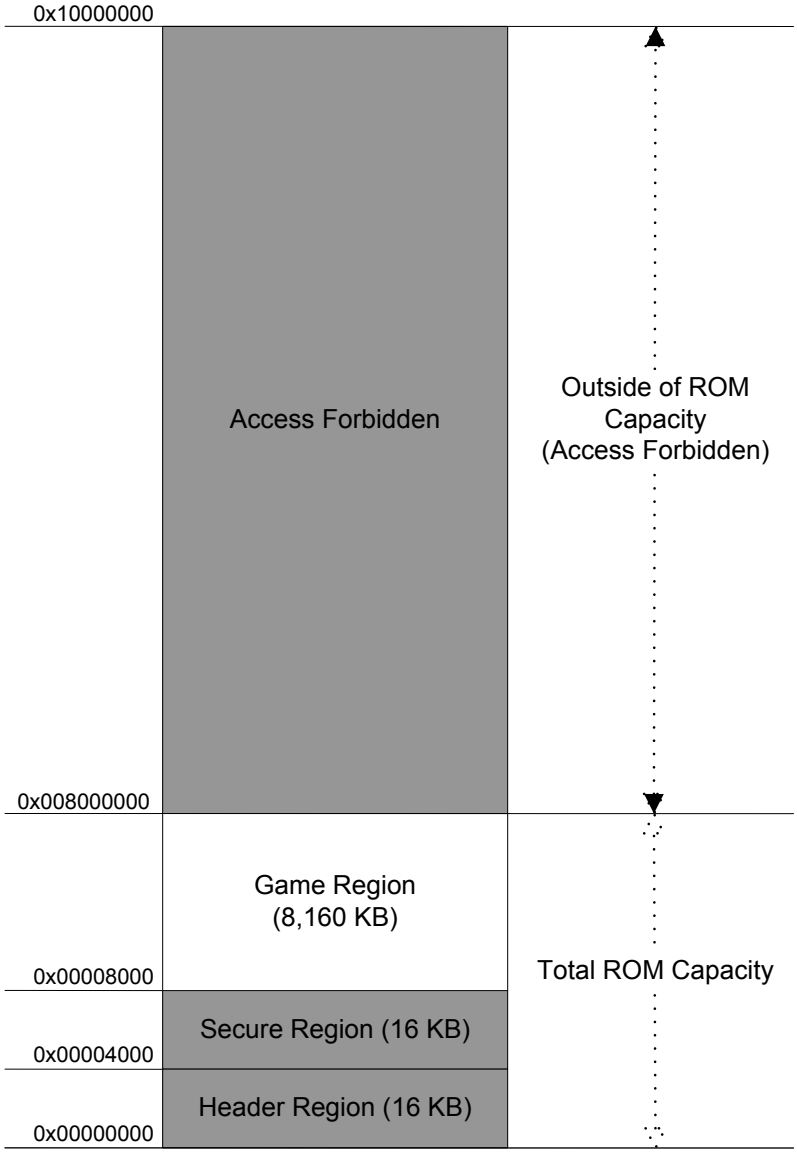
The memory map for the DS Card ROM is the same for DS units and TWL units.

- Figure 2-1 and Figure 2-2 provide examples of the memory map for a 64 megabits and a 1 gigabit, respectively.
- The address value of the game region's upper limit depends on the card's ROM capacity.

  The game region capacity is expressed as follows:

  Game region capacity = ROM total capacity – 32 KB

Figure 2-1 Memory Map for 64 Megabits (When Reading DS Card ROM with a DS Unit or TWL Unit)

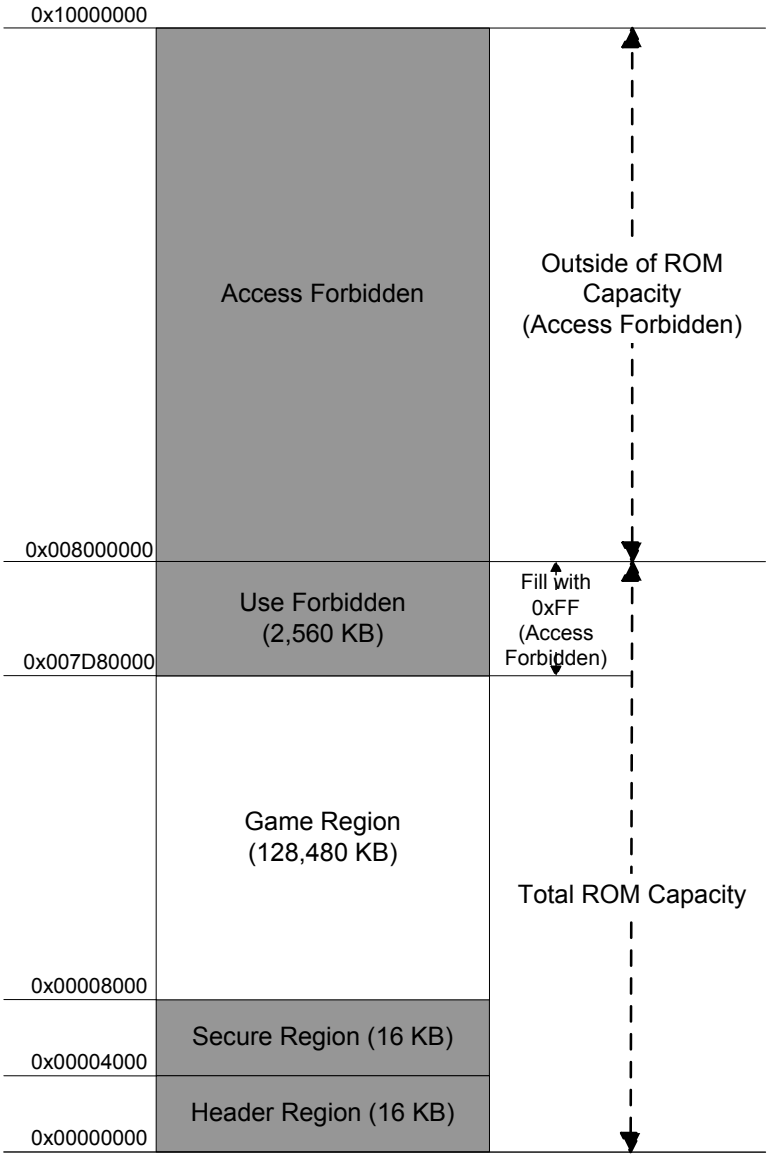


For 1-gigabit or larger, the address value of the game area's upper limit is distinct from ROMs of other capacities.

The 1-gigabit game region capacity is expressed as follows:

Game region capacity = ROM total capacity – 32 KB – 2560 KB

Figure 2-2 Memory Map for 1 Gigabit (When Reading DS Card ROM with a DS Unit or TWL Unit)



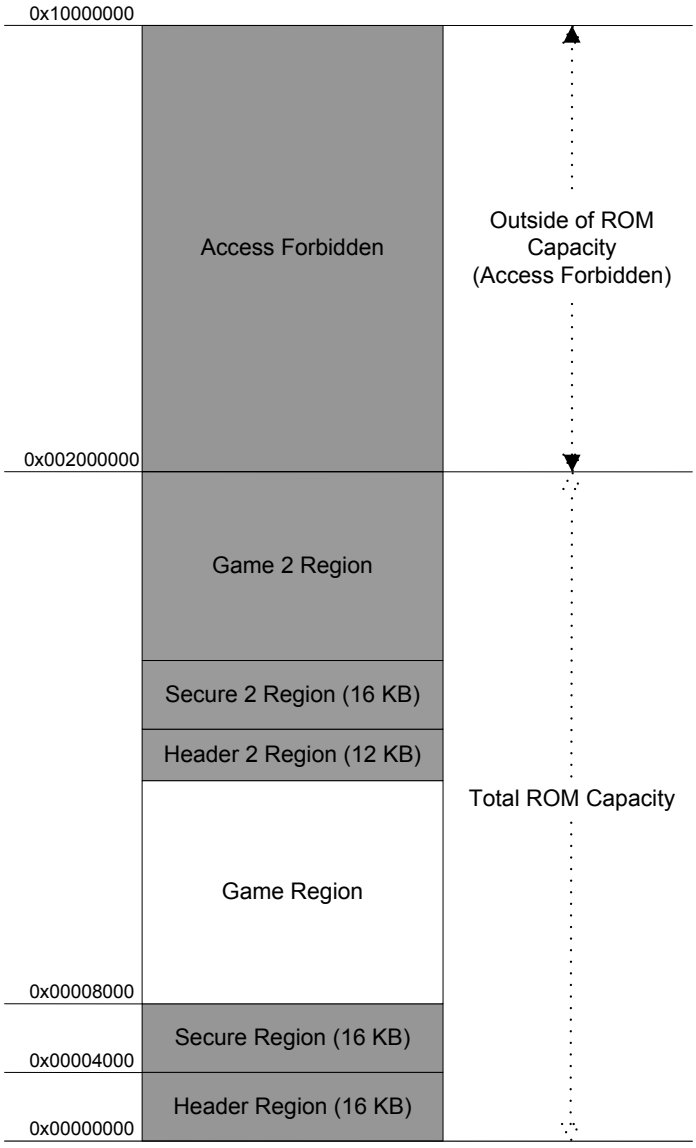
2.1.2.2 TWL-Enhanced Card and TWL Card

The TWL-Enhanced Card and TWL Card ROM places a header 2 region, security 2 region, and game 2 region after the game region. The game 2 region can be read only by the TWL unit. The Nintendo DS cannot read it. See the `makerom.TWL` reference for details on the placement method. The header 2 region start address is automatically set to 4-megabit units when the ROM image is created.

- Figure 2-3 and Figure 2-4 provide examples of the memory map for 256 megabits
- Figure 2-5 and Figure 2-6 provide examples of the memory map for a 1 gigabit
- The game region capacity is expressed as follows:

  Game region capacity = ROM total capacity – 32 KB – 28 KB – game 2 region capacity

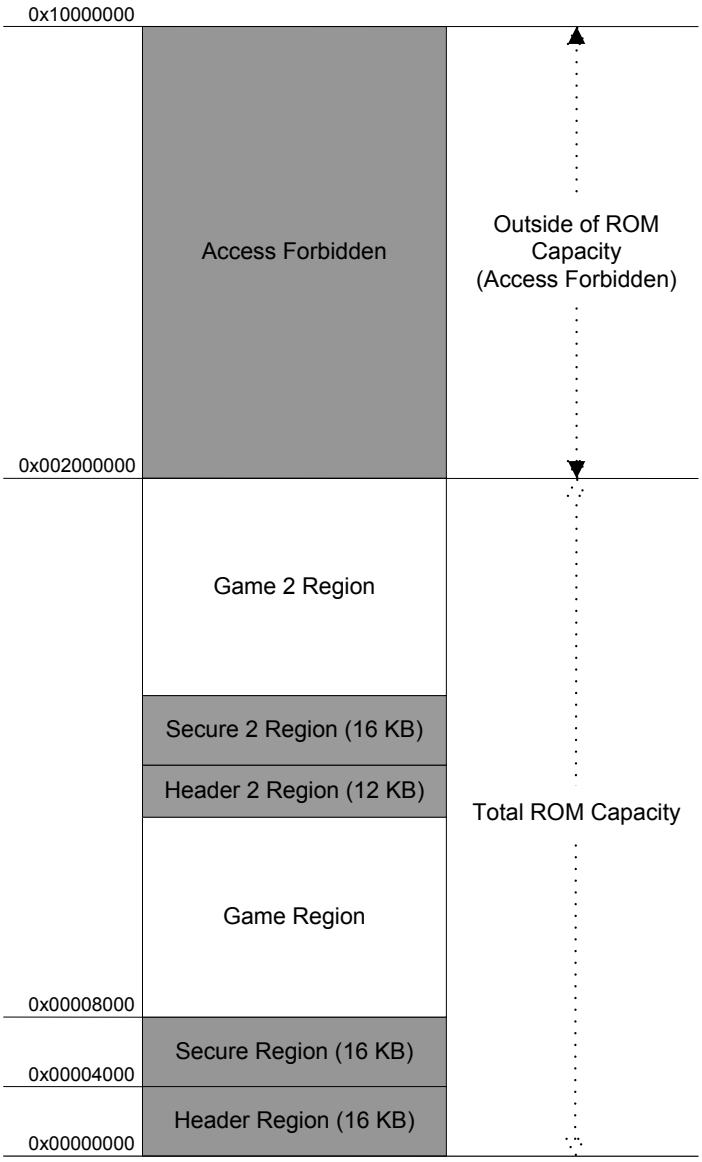
Figure 2-3 Memory Map for 256-Megabit (When Reading TWL-Enhanced Card ROM with a DS Unit)



- When reading with a TWL unit, both the game region and game 2 region can be read
- The total capacity of the game region and game 2 region is expressed as follows:

  Game region and game 2 region capacity = ROM total capacity – 32 KB – 28 KB

Figure 2-4 Memory Map for 256-Megabit (When Reading TWL-Enhanced Card or TWL Card ROM with a TWL Unit)

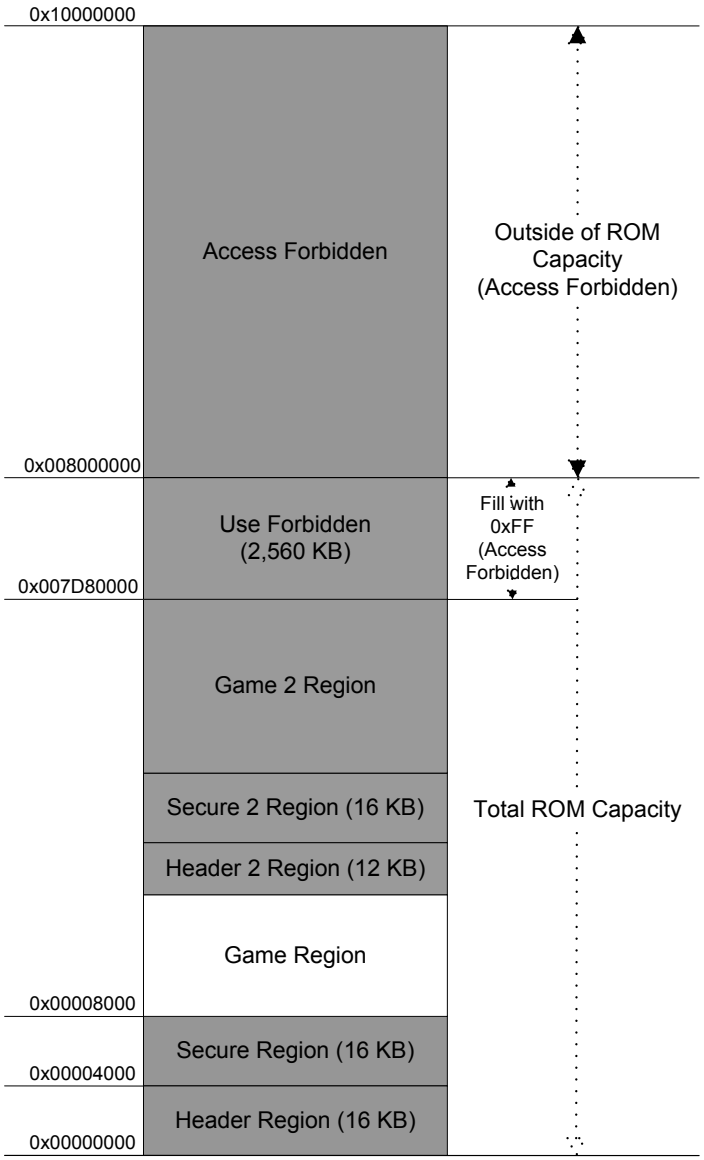


Again, for ROM, with 1-gigabit or larger, the address value of the game 2 region's upper limit is distinct from ROMs of other capacities.

The 1-gigabit game 2 region capacity is expressed as follows:

Game region capacity = ROM total capacity – 32 KB – 28 KB – game 2 region capacity – 2560 KB

Figure 2-5 Memory Map for 1-Gigabit (When Reading TWL-Enhanced Card ROM with a DS Unit)

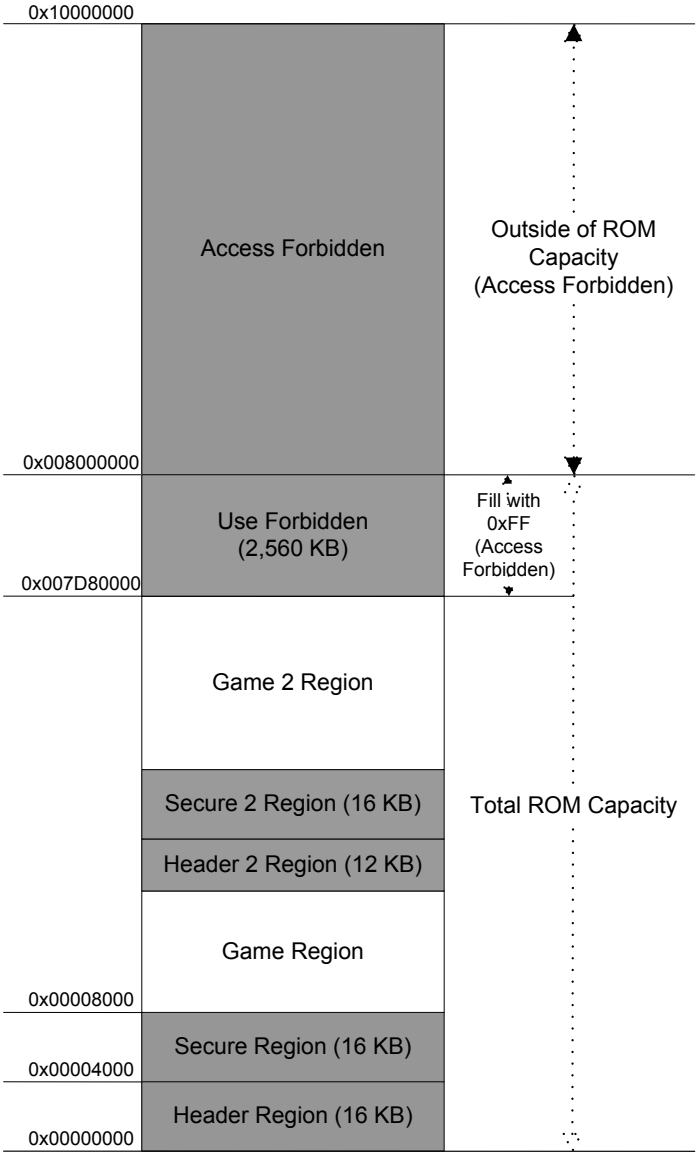


When reading with a TWL unit, both the game region and game 2 region can be read.

The total capacity of the game region and game 2 region is expressed as follows:

Game region and game 2 region capacity = ROM total capacity – 32 KB – 28 KB – 2560 KB

Figure 2-6 Memory Map for 1-Gigabit (When Reading TWL-Enhanced Card or TWL Card ROM with a TWL Unit)



2.2 Backup Memory

2.2.1 Lineup

Table 2-4 presents the lineup of backup memory devices.

Table 2-4 Lineup of Backup Memory Devices

Type of Memory	Capacity	Page Size	Number of Guaranteed Rewrites	Required Time for Rewrite (1 byte - 1 page)	Data Storage Period
EEPROM[4]	4 kilobits	16 bytes	1 million	5 ms	10 years
	64 kilobits	32 bytes			
	512 kilobits	128 bytes			
	1 megabit	256 bytes			
Flash Memory[4]	2 megabits	256 bytes	100,000 (10,000)[1]	25 ms[2] 300 ms[3]	20 years
	4 megabits				
	8 megabits		100,000	25 ms	
	16 megabits			23 ms	
	64 megabits				10 years

[1] 10,000 represents the guaranteed number of rewrites that require 25 ms each.

[2] Represents the guaranteed time for devices that have fewer than 10,000 total rewrites.

[3] Represents the guaranteed time for devices that have more than 10,000 but fewer than 100,000 total rewrites.

[4] If high-capacity 1-megabit EEPROM or high-capacity (8-, 16-, or 64-megabit) flash memory is required, please contact support@noa.com.

The following points apply to rewrite units.

- EEPROM internally maintains a one-page buffer, and rewrites are executed in chunks that range from 1 byte to one page in size.
- Low-capacity flash memory internally maintains a one-page buffer, and rewrites are executed in units of one page (for flash memory whose capacity ranges from 2 to 16 megabits).

Additional notes:

- For 64-megabit flash memory, data is erased in blocks (writing is possible in chunks as small as 1 byte).
  - 64-megabit flash: 64 KB/block
  - Write time required (1 byte to 1 page): 5 ms
  - Delete time required: 3 s

  Do not write programs that depend on erasure time. Because erasure time will be affected by individual variation among memory devices, this way of programming could lead to malfunction or the programs running out of control.